CLAIMS

What is claimed is:

1. A method comprising:

determining whether data most recently read out includes dummy data;

selectively skipping over dummy data and reading out contents of a next storage location in response to an overflow state; and

selectively reading out the most previously read out data in response to an underflow state.

2. The method of Claim 1, further comprising:

selectively reading out data of a next storage location in response to most recently read out data not comprising dummy data.

3. The method of Claim 1, further comprising:

selectively reading out data from a next storage location in response to no overflow and no underflow states.

4. The method of Claim 1, wherein the selectively skipping over dummy data comprises skipping over at least one storage location.

5. The method of Claim 1, wherein the overflow state comprises a number of addressable storage locations between subject storage locations in which write and read operations most recently took place being equal to or greater than a specified margin.

6. The method of Claim 1, wherein the underflow state comprises a number of addressable storage locations between subject storage locations in which write and read operations most recently took place being equal to or less than a specified margin.

7. The method of Claim 1, further comprising writing data into storage locations according to a first clock rate, wherein each act of reading out is based on a second clock rate and wherein the first and second clock rates differ.

8. The method of Claim 1, further comprising:

determining the occurrence of a symbol; and

providing the symbol in parallel as data available for writing into storage locations.

9. An apparatus comprising:

at least one integrated circuit, wherein the integrated circuit is to include the capability, either alone or in combination with other integrated circuits, to:

determine whether data most recently read out includes dummy data;

selectively skip over dummy data and read out contents of a next storage location in response to an overflow state; and

selectively read out the most previously read out data in response to an underflow state.

10. The apparatus of Claim 9, further comprising an integrated circuit is to include the capability, either alone or in combination with other integrated circuits, to:

selectively read out data of a next storage location in response to most recently read out data not comprising dummy data.

11. The apparatus of claim 9, further comprising an integrated circuit is to include the capability, either alone or in combination with other integrated circuits, to:

selectively read out data from a next storage location in response to no overflow and no underflow states.

12. The apparatus of claim 9, wherein the integrated circuit is to include the capability, either alone or in combination with other integrated circuits, to selectively skip over dummy data comprises the capability to skip over at least one storage location.

13. The apparatus of claim 9, wherein the overflow state comprises a number of addressable storage locations between subject storage locations in which write and read operations most recently took place being equal to or greater than a specified margin.

14. The apparatus of claim 9, wherein the underflow state comprises a number of addressable storage locations between subject storage locations in which write and read operations most recently took place being equal to or less than a specified margin.

15. The apparatus of claim 9, further comprising an integrated circuit is to include the capability, either alone or in combination with other integrated circuits, to:

write data into storage locations according to a first clock rate, wherein each act of reading out is based on a second clock rate and wherein the first and second clock rates differ.

16. The apparatus of claim 9, further comprising an integrated circuit is to include the capability, either alone or in combination with other integrated circuits, to:

determine the occurrence of a symbol; and

provide the symbol in parallel as data available for writing into storage locations.

17. A system comprising:

a first device to provide an interface with a first computing platform;

a second device to provide an interface with a second computing platform; and

an buffer device comprising at least one integrated circuit, wherein the integrated circuit is to include the capability, either alone or in combination with other integrated circuits, to:

receive data from the first device,

determine whether data most recently read out includes dummy data;

selectively skip over dummy data and read out contents of a next storage location in response to an overflow state;

selectively read out the most previously read out data in response to an underflow state; and

provide the read out data to the second device.

18. The system of Claim 17 wherein the buffer device operates in accordance with PCI express.

19. The system of Claim 17 wherein the buffer device operates in accordance with the InfiniBand Architecture.

20. The system of Claim 17, wherein the first device comprises an input/output device.

21. The system of Claim 17, wherein the second device comprises a communications standard translator.